**Date:**

**Ahsanullah University of Science and Technology**

Department of Computer Science and Engineering

Third Year, First Semester Final Examination, Spring 2016

Course No: **CSE 3109** Course Title: **Digital System Design**

Time: 3 Hours Full Marks: 70

**[ There are 7(Seven) questions. Answer any 5(Five) questions.]**

**[*Marks allotted are indicated in the right margin within ‘[ ]’.*]**

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| --- | --- | --- |
| 1.a) | What is Register? What are the differences between SRAM and DRAM? | [3] |
| b) | Show all the steps of Booths algorithm for the following 6 bit numbers:  X= -8 Y = -9 | [5] |
| c) | Design a 5 × 5 bit booth’s multiplier. Draw the circuit block diagram. | [6] |
| 2.a) | What is Arithmetic Logic Unit? | [2] |
| b) | What is PLA? What are the differences between PLA and ROM? | [3] |
| c) | Design a 4-bit binary counter by using J-K flip flops. | [4] |
| d) | Describe the effect of output carry for the following arithmetic operations.   |  |  |  |  | | --- | --- | --- | --- | | S1 | S0 | Cin = 0 | Cin = 1 | | 0 | 0 | F = A | F = A + 1 | | 0 | 1 | F = A + B | F = A + B + 1 | | 1 | 0 | F = A – B – 1 | F = A – B | | 1 | 1 | F = A – 1 | F = A |   Consider all inputs contain **n** bits. | [5] |
| 3.a) | Determine the truth table, map simplification and PLA program table for the following two functions:  F1 = ( B’C’ + A’C’ + A’B’ )’  F2 = B’C’ + A’C’ + ABC | [4] |
| b) | Prove that the multiplication of two **n-digit** numbers in any base **r** gives a product of no more than **2n** digits in length. | [4] |
| c) | Deign an arithmetic logic unit with two selection variables S1 and S0, that generates the following arithmetic and logic operations.   |  |  |  |  |  | | --- | --- | --- | --- | --- | | S1 | S0 | Cin = 0 | Cin = 1 | Cin = × (don’t care) | | 0 | 0 | F = A + B | F = A + B + 1 | F = A+B (OR) | | 0 | 1 | F = A | F = A + 1 | F = A⊕B (XOR) | | 1 | 0 | F = B’ | F = B’ + 1 | F = AB (AND) | | 1 | 1 | F = A + B’ | F = A + B’ +1 | F = A’ (Complement A) | | [6] |
| 4.a) | Write a program for SAP-1 to solve the given arithmetic problem and then translate the program into SAP-I machine language.  16 + 20 + 24 – 32  The numbers are in decimal form. | [4] |
| b) | Describe the architecture of SAP-2. | [5] |
| c) | Draw the OUT and SUB routines of SAP-1 and also draw their fetch and execution timing diagram. | [5] |
| 5.a) | What is mnemonics? Explain with example. | [2] |
| b) | What is Ring Counter? Draw the symbol and clock and timing signals of a Ring Counter. | [3] |
| c) | How much time delay does this SAP -2 subroutine produce?  MVI A,0AH  LOOP1: MVI B,64H  LOOP2: MVI C,47H  LOOP3: DCR C  JNZ LOOP3  DCR B  JNZ LOOP2  DCR A  JNZ LOOP1  RET | [4] |
| d) | The traffic lights on a main road show green for 50 s, yellow for 6 s, and red for 30 s. Bits 1, 2 and 3 of port 4 of SAP-2 are the control inputs to peripheral equipment that runs these traffic lights. Write a program in mnemonics for SAP-2 that produces time delays of 50, 6 and 30 s for the traffic lights. | [5] |
| 6.a) | What is the difference between hard-wired control and microprogram control? What are the advantage and disadvantage in each method? | [4] |
| b) | Design a hard-wired control to implement the addition and subtraction of two fixed-point binary numbers represented in sign magnitude form. Your design must include the following steps:   1. Equipment Configuration 2. Derivation of the Algorithm 3. Flowchart 4. Control state diagram and Sequence of microoperations 5. Design of Hard-wired Control   You must use an ALU that has the following function table:   |  |  |  |  |  | | --- | --- | --- | --- | --- | | S2 | S1 | S0 | Cin | Output | | 0 | 0 | 1 | 0 | F = A + B | | 0 | 1 | 0 | 1 | F = A - B | | 1 | 1 | 1 | 0 | F = A’ | | 0 | 0 | 0 | 1 | F = A + 1 | | [10] |
| 7. | **Figure 1:** control state diagram for question no. 7  z = 0    x = 0 x = 1 y = 1    y = 0      z = 1 |  |
|  | The state diagram of a control unit is shown in Figure 1. It has eight states and three inputs x, y and z. |  |
| a) | Design the control using eight D flip-flops. | [4] |
| b) | Design the control using three J-K flip-flops and a 3×8 decoder. | [5] |
| c) | Design the control using a PLA. | [5] |